ABSTRACT OF THE DISCLOSURE

A data line driving circuit 200 has a shift resistor unit 210 in which respective shift resistor unit circuits Ua1 to Uan+2 are in cascade connection with each other, and an output signal control unit 220 comprising respective operational unit circuits Ub1 to Ubn+1. A NAND circuit 514 controls an enabling period of a negative sampling signal based on an output signal from a NAND circuit 511 in an subsequent-stage operational unit circuit.